

SECTION 1

Hardware Overview

1.1 INTRODUCTION

1.1.1 Explorer Processor.

The purpose of this section is to supply the reader with sufficient knowledge of the processor so that the terminology in the following sections can be understood. This section does not attempt to explain all there is about the processor. If the reader wants to know in detail about the processors, he or she should read the manuals SPECIFICATION: EXPLORER PROCESSOR, part number 2236414-0001 and/or SPECIFICATION: EXPLORER II PROCESSOR, part number 2540834.

There are two types of processor: The Explorer I and the Explorer II. The main difference in the two is that the Explorer I (the original processor) is implemented on a board and the Explorer II is implemented on a chip. There are other differences, but this section only deals with the common features.

The function of the processor is to execute code called microcode. An overview of microcode will be discussed later.

1.1.2 Explorer Buses and Components.

The internals of the Explorer processor appears to be an almost general purpose computer. Inside the Explorer there is memory and special registers which are manipulated by the microcode instructions. The memory and special registers are located on one of several buses which exist in the processor. The three major buses found in the processor are the A-Bus, the M-Bus, and the O-Bus.

1.1.2.1 The A-Bus.

The A-Bus has only one component which is a block of memory. The memory size is 1K by 32-bit words - this notation means 1K block of 32 bit words. The first 64 words of this memory block are special and will be discussed in the section on the M-Bus. (There is another component on the A-Bus, but it is transparent

to the microcoder and its purpose is to speed up accesses to and from the memory on the A-Bus.) The memory on the A-Bus is referred to as the A-Memory.

1.1.2.2 The M-Bus.

The M-Bus has many components on it. Only a few will be discussed.

M-Memory.

On the M-Bus there is a block of memory whose size is 64 words by 32-bits. This memory is referred to as M-Memory. The first 64 words of A-Memory are an exact image of M-Memory. That is, if microcode writes to location 5 of M-Memory, then location 5 of A-Memory also gets changed to image location 5 of M-Memory.

The PDL, PDL Pointer, and PDL Index.

PDL means Push Down List. The PDL is a cache stack of 1K by 32-Bit words. The PDL Pointer and PDL Index are both components on the M-Bus. The PDL Pointer points to the top of the stack (TOS). The PDL Index can be modified to point anywhere in the stack. Like any other stack, data can be pushed onto it or popped off it. It should be noted that the Lisp microcode uses the cache PDL as a cache portion of a larger PDL which resides in NuBus memory.

The MD Register.

The MD register is a 32 bit register. It can be thought of as the processor's window. When data is read from outside the processor it comes into the MD register. When data is to be written outside the processor, it is first placed into the MD register.

The VMA Register.

The VMA register works in conjunction with the MD. MD holds what is read or to be written and the VMA holds where the external data is to be read from or to be written to.

There are other components on the M-Bus, but these are not discussed in this document. See one of the specifications listed earlier for more details.

The O-Bus.

There is a component in the processor called the Arithmetic Logic Unit (ALU). Its function is to take data from the M-Bus and the A-Bus and perform arithmetic or logical operations on that data (like addition). When the ALU performs that operation, it puts the result on the O-Bus. The O-Bus in turn selects which

component to store the result in. A- and M-Memory are both on the output side of the O-Bus along with M-Bus registers like MD or VMA. This means the O-Bus can select these components to store its data in.

1.1.3 Microcode.

1.1.3.1 I-Memory.

I-Memory is another memory block in the Explorer processor. I-Memory is used to store the microcode instructions. The size of I-Memory on the Explorer I is 16K by 56-Bits. The size of I-Memory on the Explorer II is 32K by 64-bits. I-Memory is sometimes referred to as Writable Control Store or WCS.

1.1.3.2 Instructions.

Microcode has a lot of similarity to assembly language in that it is very close to the actual architecture of the machine. There are four basic types of microcode instructions, but there are many ways to augment each instruction type. The four types are

- The ALU instruction. This instruction type allows the microcoder to perform arithmetic or logical instructions on an A-Memory value and an M-Memory value or an M-Bus register and store the results into a specified destination.
- The Byte Instruction. This instruction type allows the microcoder to take a specified portion of an M-Memory Word or M-Bus Register and deposit it into an A-Memory word and then place the result into a specified destination.
- The Jump Instruction. The Jump instruction can take on many forms with augmentation. For example, the Jump instruction can do a conditional or unconditional Jump; it can conditionally or unconditionally return from a subroutine call; and, it can conditionally or unconditionally perform a subroutine call.
- The Dispatch Instruction. The Dispatch instruction is something like a Jump instruction; however, its destination is not located in the instruction, but rather in a table called the dispatch table. This table is located in special memory on the M-Bus called Dispatch Memory. The Dispatch instruction uses an M-Bus source as an index into the table. Control then jumps or calls the instruction whose address is in that

particular location in Dispatch Memory.

1.1.3.3 Labeling Conventions.

There are labeling conventions for A- and M-Memory. If a label is assigned to an A-Memory location, it begins with the characters 'A-'. So a temporary location in A-Memory might be labeled A-TEMP. The corresponding convention is true for M-Memory labeling. An M-Memory location might be called M-SAVE. The reason this is important to the reader is that certain M-Memory and A-Memory locations have special meaning to the Lisp microcode and are referenced in this document. An example is the location A-BOOT-COMMAND-BLOCK which is a flag to the Lisp microcode just after booting occurs.

1.2 MAJOR COMPONENTS

The Explorer system consists of three major hardware components: the system enclosure, the monitor, and the mass storage subsystem. It is expected that over time additional components and peripherals will be added to form a broad family of compatible systems.

1.2.1 System Enclosure.

The system enclosure consists of a seven-slot card chassis housed in a low profile cabinet that fits under a desk. The backplane for the chassis provides the vehicle for all I/O connections and contains a NuBus for board-to-board interconnection. The cabinet also contains a power supply and provides two switched outlets for the monitor and mass storage unit.

1.2.2 Brief Descriptions of Each Board.

Explorer processor

- Explorer I - 500-IC microcoded Lisp engine
- Explorer II - Lisp engine containing Lisp microprocessor chip
- Two-level, demand-paged virtual memory map
- Self-test ability
- Private bus (local bus) to Explorer memory board and graphics display (Explorer I only)

Explorer memory board

- 2mb, 4mb, 8mb, 16mb, 32mb versions with byte parity
- Two ports - NuBus and the Explorer private bus (on 2, 4 and 8mb boards)
- Interfaces Explorer processor to NuBus
- Read-only memory (ROM) contains board identification information and extensive board diagnostics

System Interface board (SIB)

- Time of day and interval timers
- Non-volatile memory (NVRAM) - the NVRAM is a 2kbyte stable storage RAM on the system interface board. It is used during system testing and booting to locate resources and later for storing and retrieving a variety of other information.
- Monitor, keyboard and mouse controls
- RS-232C port and an eight-bit parallel port
- ROM containing board identification, board diagnostics, and generic device drivers for the monitor and keyboard

NuBus Peripheral Interface (NUPI) board

- NuBus to SCSI intelligent adaptor
- Extensive self-test
- ROM contains board identification information and system load device driver

Local Area Network (LAN) board

- Ethernet 10 MHZ interface
- Extensive on-board packet buffers directly accessible via NuBus
- ROM containing board identification information, diagnostics, and system load device driver.

1.2.3 Monitor.

The landscape black and white monitor is connected to the system enclosure via a dual fiber-optic cable, allowing placement of the monitor remote from the system enclosure. The keyboard and mouse connect to the front of the monitor. The mouse provides rapid, smooth cursor movement and positioning using a 200 dots per inch optical pad.

1.2.4 Mass Storage Subsystem.

The mass storage subsystem provides two 5 1/4" envelopes, power, and cooling for the mass storage system. Winchester or cartridge tape components may be inserted in either of these two envelopes.

Connection to the system enclosure is via an SCSI interface cable.

1.3 INTRASYSTEM COMMUNICATION

The system backplane provides three connectors (P1, P2, and P3) per slot. These three connectors are used for all connections to the board. There are no front edge connectors. The backplane dedicates connector P1 as the NuBus, the primary system bus. P2 is used for the local bus on certain slots, and is available for general I/O on other slots. P3 is a general I/O connector on all slots. The configuration of the backplane is shown in Figure 1-1.

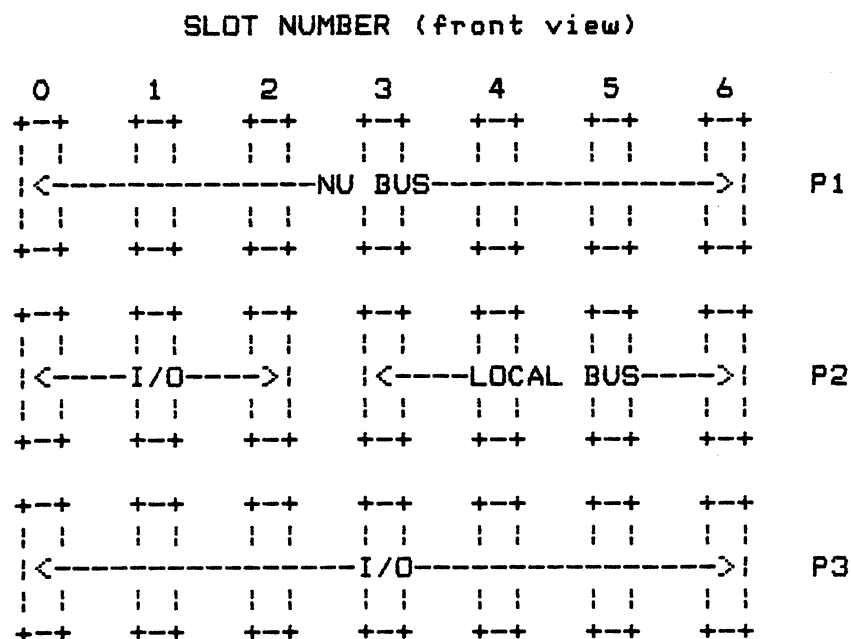


Figure 1-1 Backplane Configuration

1.3.1 NuBus.

The NuBus is the primary mechanism for board-to-board communication. The NuBus is a 32-bit system bus on which the address and data lines are multiplexed onto the same lines. All control, data and power lines are defined so as to fit through one 96 pin DIN connector. On the Explorer backplane, connector P1 is reserved in all slots for the NuBus.

Data may consist of 8 bits (one byte), 16 bits (one halfword), or 32 bits (one word). The bit and byte numbering scheme is referred to as little endian in which both the lowest numbered bit and byte is the least significant. Bytes, halfwords, and words are organized as shown in Figure 1-2.

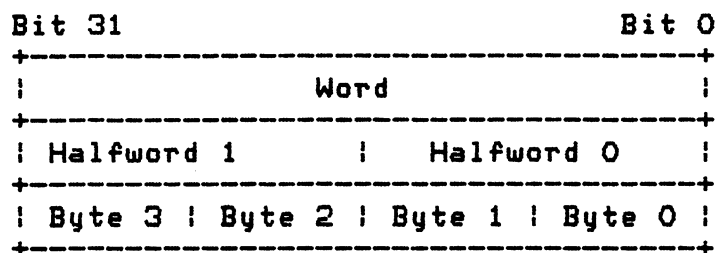


Figure 1-2 Layout of Words, Halfwords, and Bytes

The NuBus spec leaves some areas open or subject to interpretation for a given system. The following paragraphs define these areas as they apply to the Explorer system.

1.3.1.1 Block Moves.

The ability to perform block moves as defined by the NuBus spec is required on any large block of memory that may be considered a system resource. Small blocks of memory used as a buffer on a peripheral controller or a block of memory used only as a private memory and located in the control address space need not support block moves. All boards indicate via the ID ROM flags the presence or absence of block support on that board. On the Explorer only the memory board supports slave block moves.

1.3.1.2 Time-Out Period.

The bus time-out period for the Explorer is fixed at 25 microseconds (ms).

1.3.1.3 Parity.

Bus parity is not generated or checked by any Explorer component board.

1.3.1.4 Reset Operation.

On power-up, the source (the System Interface Board) that drives the RESET/ signal will hold it active (low) for at least 100 ms to guarantee the correct startup of certain MOS devices. After RESET/ goes inactive (high), all boards that execute self-tests will proceed with their tests.

RESET/ may be driven low at any time by any device to cause a system restart. This would typically be done by a "deadman" timer option or a remote diagnostic option. In this case, all boards will execute self-test and the system will reboot. RESET/ must be low for two or more clock cycles to force the system restart.

1.3.1.5 Power Fail.

The System Interface Board posts a power fail event to those boards that need a power fail warning. Software must program the SIB with the specific addresses for power fail events.

1.3.1.6 System Addressing.

Starting addresses for the boards are determined by slot location. In hexadecimal form, this address is >FS000000 (sometimes appears as F(ID)000000). The most significant hexadecimal digit, F, is the largest hexadecimal number, corresponding to binary 1111. The next digit, S, is the slot number given in hexadecimal. The remaining six zeros are hexadecimal digits, each corresponding to binary 0000.

1.3.1.7 Configuration (ID) ROM.

Each board has an ID ROM that describes the basic characteristics of that board. This ROM may be accessed at addresses F(S)FFFFFF - F(S)FFFF00 for any and all slot ID's. The ID ROM contains 64 or more bytes of information about each board, such as: serial number, part number, and board type. This ROM resides at the highest address of control space on each board and supplies one byte of data (byte 0) for each word address.

1.3.1.8 Bus Locking.

No bus master will lock the bus for more than five contiguous single-word transfers or one 16-word block transfer. However, during power fail, the bus may be locked to quickly post power-fail events.

1.3.1.9 NuBus Clock.

The System Interface Board that drives the NuBus clock line makes provision to disable that clock output so that two such cards may be installed.

1.3.1.10 Unimplemented Memory.

When a board recognizes an address that is within its control space but it has no memory at that address, it may either:

- * Return ACK with timeout status
- * Do nothing and allow the system watchdog to generate a timeout

1.3.1.11 Byte, Halfword, and Word Transfer Protocols.

The following bus protocols prevent unnecessary problems on bus transfers:

1. Slaves that provide only a byte interface position this byte in the least significant byte position (byte 0) of the NuBus word. Consecutive bytes appear in consecutive NuBus words, always at the byte 0 position. A master may read or write the slave using byte, halfword, or word operations. Data in any positions other than byte 0 must be ignored.
2. Slaves that provide only a 16-bit halfword interface position this in the least significant halfword position (halfword 0) of the NuBus word. A master may read or write the slave using byte, halfword, or word operations. Data in positions other than halfword 0 (bytes 0, 1) must be ignored.
3. Slaves that provide a full 32-bit word interface perform byte, halfword or word transfers.

With these guidelines, a master that can do only word transfers can communicate with any slave device. A master that is limited to byte or halfword transfers cannot talk to word-only slaves. All NuBus masters should have word transfer capability. Design of masters without 32-bit word capability is strongly discouraged.

1.3.2 Explorer Bus (Local Bus).

The Explorer Bus is a high-speed bus for private communication between one master and one or more slaves, such as a processor/memory board set. One Explorer bus is provided on the backplane using connector P2 of slots 3, 4, 5, and 6. An Explorer must have a memory board in slot 4 in order for the processor to boot. The memory interface logic is hardwired to slot 4. An additional Explorer bus or buses may be added by connecting two or three connectors together with a cable or

adapter board on the back side of the backplane. The Local Bus is used only by the Explorer I.

1.3.3 I/O Connectors.

Certain pins of P1, P2, and P3 are dedicated to power and ground functions.

1.4 INTERSYSTEM COMMUNICATION

All intersystem or external I/O connections are made from the back side of the backplane. Fiber optic links are the preferred method of interconnecting the system boxes to minimize radio frequency interference and electrostatic discharge effects and to reduce cable crowding.

The monitor to system chassis link carries video and audio data to the monitor, and receives audio, keyboard, and mouse information from the monitor.

The mass storage to system chassis link carries data and commands to and from the mass storage box.

At least one RS-232C interface and one eight-bit printer interface are provided on each system for low cost peripheral connection.

1.5 EXPLORER SYSTEM DEFINED ADDRESSES

While the Explorer system is based on the notion of dynamic configuration, several items must be fixed in order for the system to establish initial operation. Table 1-1 defines these fixed items.

Table 1-1 System-Defined Addresses

Address	Description
F6E00000	Explorer power fail event.
F6E00004 !! F6E0003C	All hardware-decoded interrupt events, except power fail, will fall within these addresses. The byte written to any interrupt even address must contain a 1 in bit 0. The remaining bits are reserved for future use and should also be set to 1.
FS000000	Starting address of memory that may be used by the system for general purpose, as indicated in the ROM flag register. This is the least significant byte of the memory block.
FSFFFF00 !! FSFFFFFF	Configuration ROM, first 64 bytes. Larger configuration ROMs will occupy the contiguous space below these addresses.
F(SIB)Fxxxx	Bus timeout address. Nothing shall respond to this address, so a read or write at this address tests timeout generation.